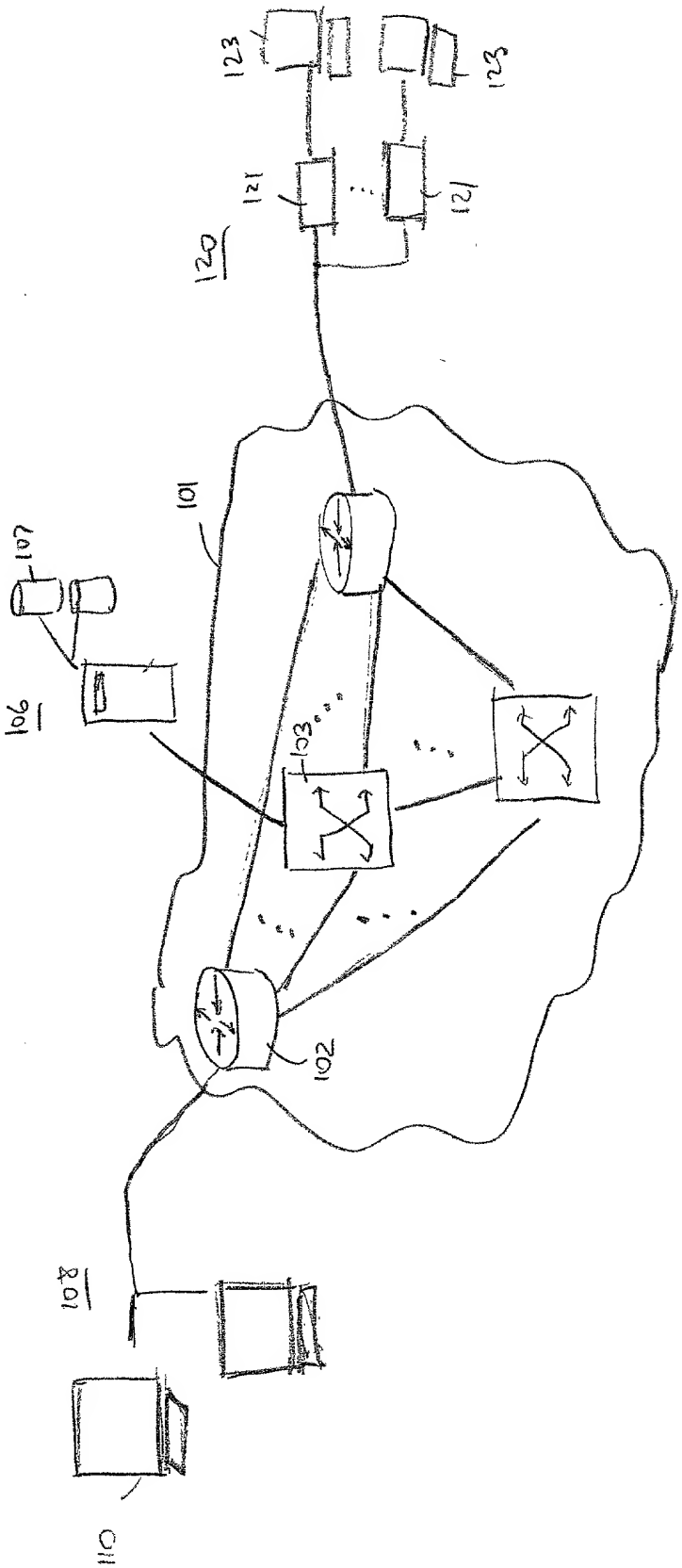


FIG. 1

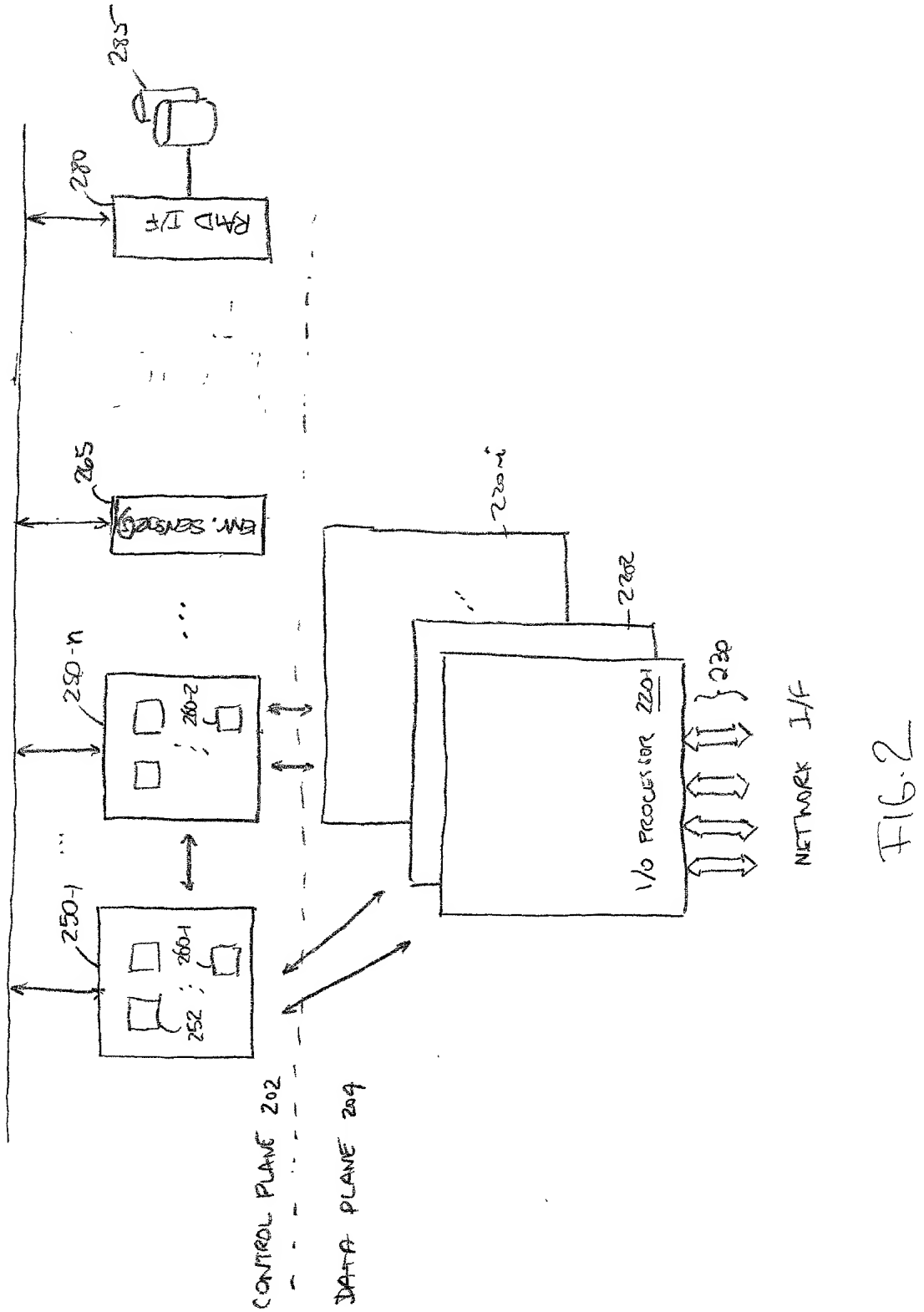

200
285
280
RMD I/F
265
ENV. SENSORS
250-n
260-2
250-1
260-1
252
220-1
222
220
I/O PROCESSOR 221
NETWORK I/F
CONTROL PLANE 202
DATA PLANE 204
102, 103

FIG. 2

System Card Interconnect

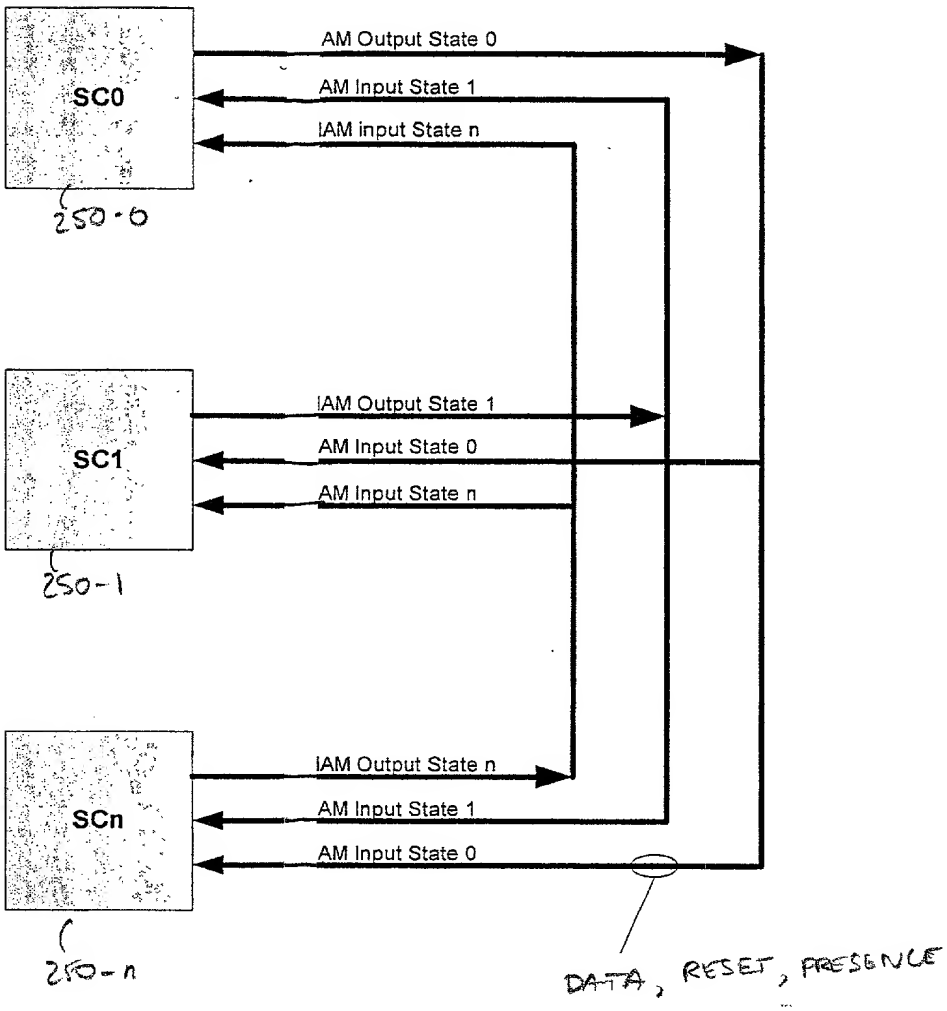


FIG. 3

T09T60" TTZhS660

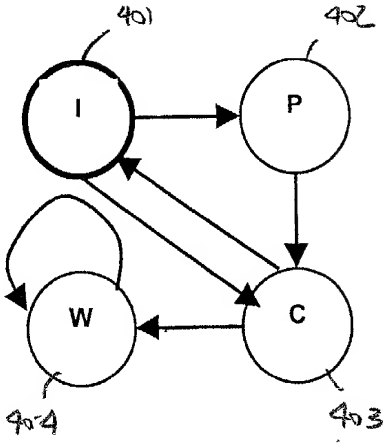


FIG. 4

Transitions

I => P (more than one cpu card is present)

I => C (only one cpu card is present)

P => C (the Pause State duration expired)

C => I (temporary/committed identity conflict encountered)

C => W (identity committed to master-write register)

W => W (wait for event)

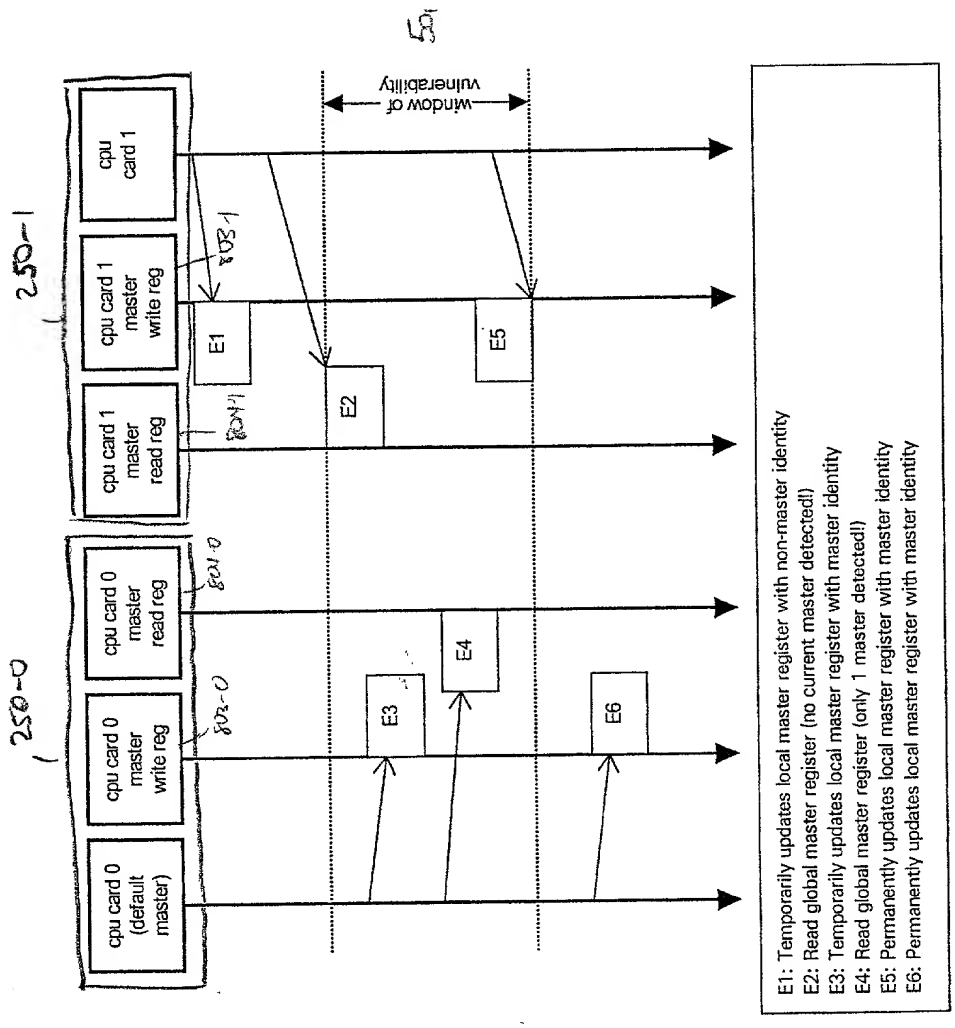

250-0
250-1
cpu card 0 (default master)
cpu card 0 master write reg
cpu card 0 master read reg
cpu card 1 master write reg
cpu card 1 master read reg
cpu card 1
window of vulnerability
E1
E2
E3
E4
E5
E6
E1: Temporarily updates local master register with non-master identity
E2: Read global master register (no current master detected!)
E3: Temporarily updates local master register with master identity
E4: Read global master register (only 1 master detected!)
E5: Permanently updates local master register with master identity
E6: Permanently updates local master register with master identity

FIG. 5

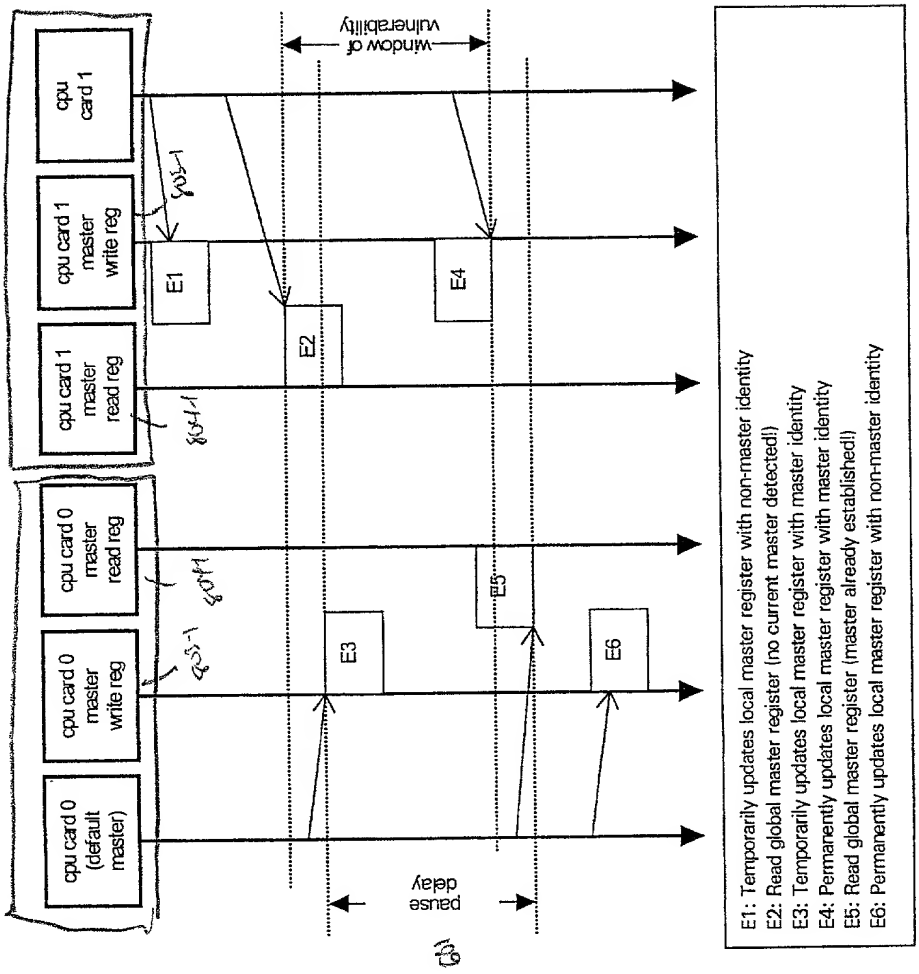
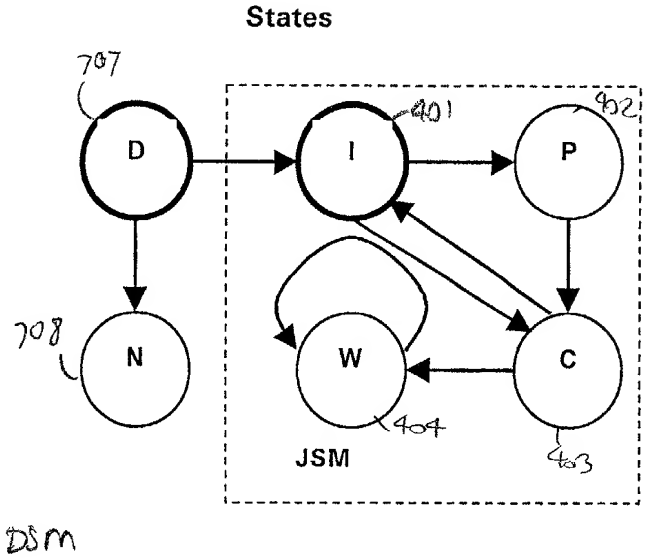

250-0
250-1
cpu card 0 (default master)
cpu card 0 master write reg
cpu card 0 master read reg
cpu card 1 master read reg
cpu card 1 master write reg
cpu card 1
E1
E2
E3
E4
E5
E6
window of vulnerability
pause delay
E1: Temporarily updates local master register with non-master identity
E2: Read global master register (no current master detected!)
E3: Temporarily updates local master register with master identity
E4: Permanently updates local master register with master identity
E5: Read global master register (master already established!)
E6: Permanently updates local master register with non-master identity

FIG. 6

TO8T60" TTZh5660



Transitions

D => I (departed card was current master)

D => N (departed card was not current master)

FIG. 7.

801

Bit field	R/W	Default	Function
0	R/W	0	SC Master state
31:2	R/w	0x0000000	Reserved

SC Master Register

FIG. 8A

802

Bit field	R/W	Default	Function
0	R	0	SC0 present
1	R	0	SC1 present
n	R	0	SCn present
31:n+1	R	0x0000000	Reserved

SC Slot Presence Register

FIG. 8B

803

Bit field	Host R/W	Default	Function
7:0	R/w	0x00	Software specified
31:8	R	0x000000	Reserved

AM Master Write Register

FIG. 8C

804

Bit field	Host R/W	Default	Function
7:0	R	0x00	RSC ... AM state (software specified)
31:8	R	0x00000	Reserved

AM Master Read Register

FIG. 8D

805
806
807

Bit field	Host R/W	Default	Function
0	*W/R*	*0x0*	*AM Receive Data Interrupt*
1	*R*	*0x00000*	*AM Reset Interrupt (RSC has been reset)*
2	*R*	*0x00000*	*AM Slot Change Interrupt (RSC inserted or extracted)*
31:8	R	0x0000000	Reserved

AM Interrupt Status Register

FIG. 8E

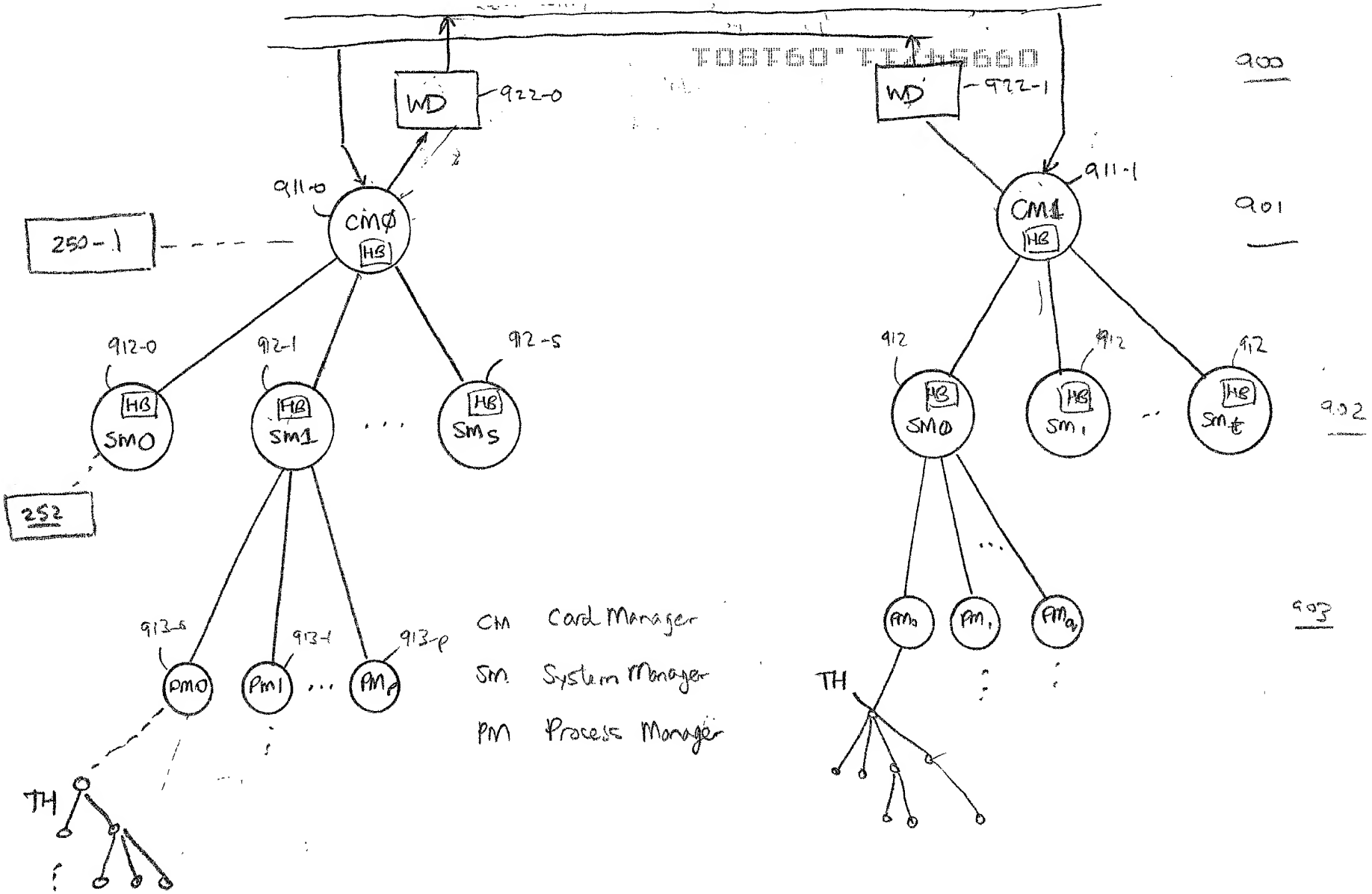
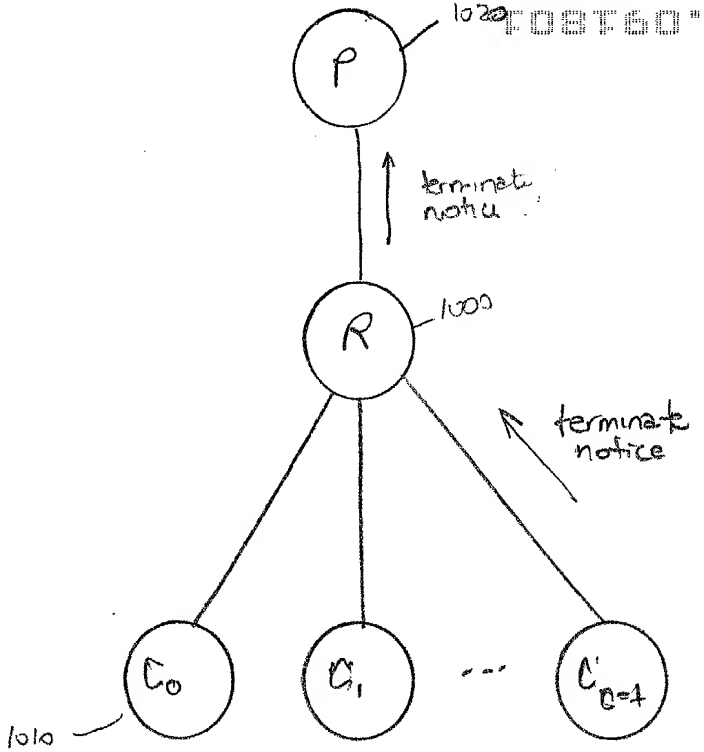


FIG. 9 Availability Manager (AM) Software Hierarchy

Docket/App No.: 3085.1000-004
Title: System Resource Availability Manager
Inventors: Arthur Zaifman, et al.



- Responsibility of R terminates at N
- R depends on C for terminate notice
- if R cannot restart C, sends terminate notice to P

R = CM, SM, PM

C = SM, PM, TH

P = WD, CM, SM

FIG. 10

Express Mail Label No. EV 339955 745 US

$R_n = CM, SM$

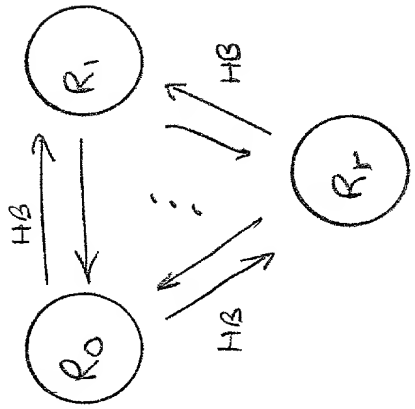


FIG. 11

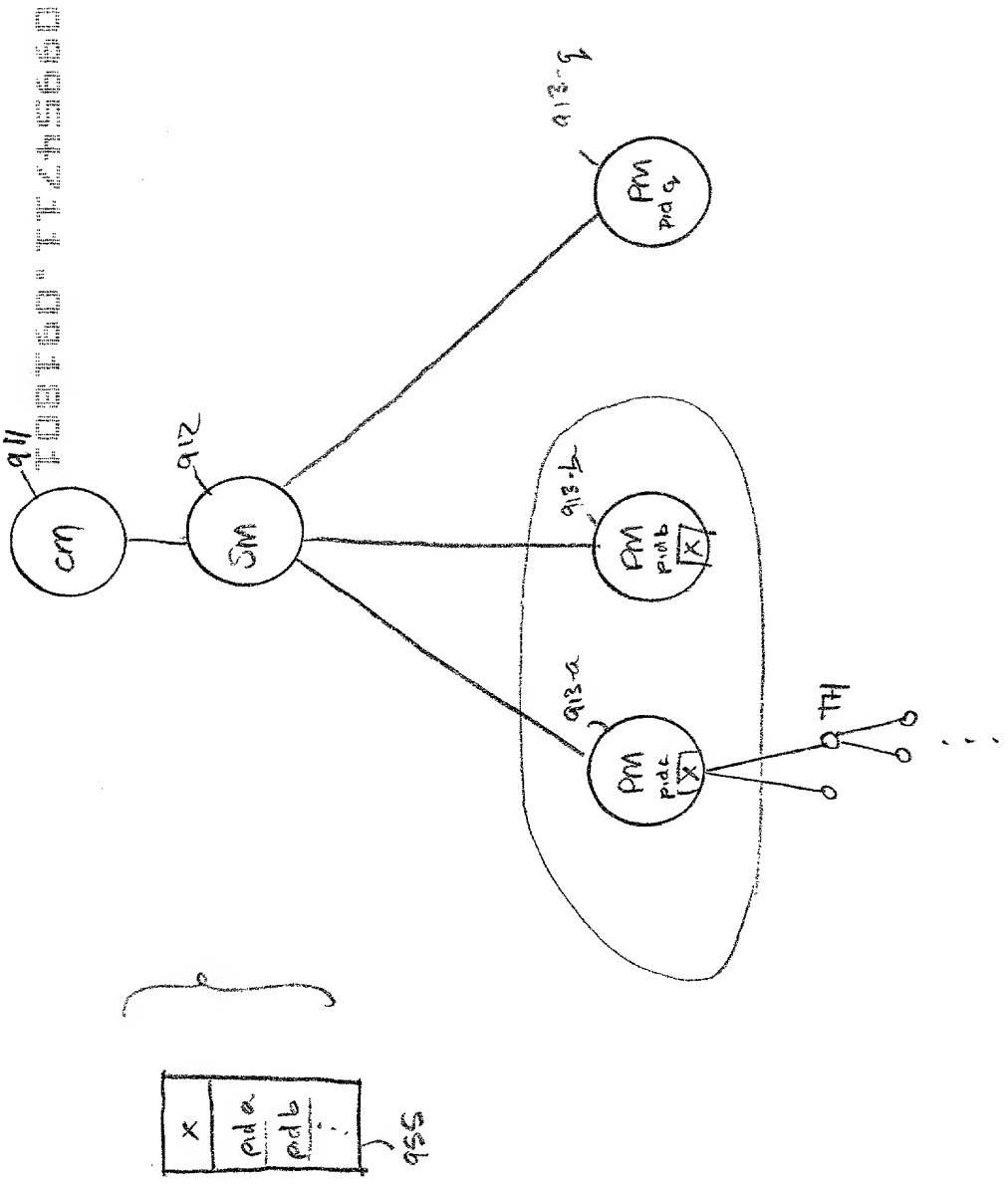

911
CM
912
SM
913-a
PM
pid a
913-b
PM
pid b
X
913-g
PM
pid g
TH
955
X
pid a
pid b

FIG. 12